Repairable Finite State Machines

ABSTRACT OF THE DISCLOSURE:

A method and respective hardware logic circuit for implementing partially programmable Finite State Machines in the hardware of digital systems which use finite state machines to implement the control logic of the hardware design. In order to provide a partly reprogrammable Finite State Machine (FSM), which can be reprogrammed in a limited way such that no costly new physical re-build of the chip including said FSM is required, a hardwired FSM includes circuit means that allow that each hardwired product term to be disabled, and further includes means that add programmable product terms which allow adding new behavior to the state machine. Scan-Only SRLs are preferably used to program the required behavior of those programmable product terms.